<center>**REMARKS/ARGUMENTS**</center>

In the Office Action, the Examiner noted that claims 1-82 are pending in the application. The Examiner additionally stated that claims 1-82 are rejected. By this amendment, claims 1-4, 6-10, 17, 19-22, 27, 39, 58-59, 67-70, 74, and 79 have been amended, and new claims 83-113 have been added. Hence, claims 1-113 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

Applicant has amended the title to more accurately identify the subject matter of the invention. No new matter is presented.

In the Claims

Rejections Under 35 U.S.C. §102(e) and Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claims 23-28, 30-40, and 79 under 35 U.S.C. 102(e) as being anticipated by Beukema et al., US 2002/0073257 (hereinafter, *Beukema*). The Examiner also rejected claims 1-22, 41-78, and 80-82 under 35 U.S.C. 103(a) as being unpatentable over *Beukema*, in view of "Building Up Chips Using VHDL and Synthesis", by Doug Warmke, (hereinafter *Warmke*). The Examiner also rejected claim 29 under 35 U.S.C. 103(a) as being unpatentable over *Beukema*, in view of what is well-known in the art. Applicant respectfully traverses the Examiner's rejections.

According to MPEP 706: "The goal of examination is to clearly articulate any rejection early in the prosecution process so that the applicant has the opportunity to provide evidence of patentability and otherwise reply completely at the earliest opportunity." According to 37 CFR 1.104: "When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained." Applicant respectfully asserts that, for many elements and limitations of the claims, Applicant cannot determine from the Office Action of

11/18/2005 or from the Office Action of 7/14/2006 which elements of *Beukema* the Examiner believes correspond to the claim elements and how the elements of *Beukema* function according to the limitations claimed. For each claim, the Examiner broadly refers to whole paragraphs of *Beukema* without specifically indicating which elements are intended to correspond to the claim elements.[1] On March 22, 2006, Applicant's undersigned representative spoke on the telephone with the Examiner's supervisor, BUNJOB JAROENCHONWANIT, regarding the difficulty of responding to the Office Action, who advised Applicant's representative to attempt to reply to the Office Action to the extent possible. Applicant's amendment of 4/18/2006 specified the assumptions of which elements of *Beukema* the Examiner intended, and traversed the rejections based on the assumptions. Where these assumptions were incorrect, or where Applicant was unable to make an assumption, Applicant respectfully requested the Examiner to designate the particular part of *Beukema* relied upon as anticipating the limitations of the claims, in order to provide Applicant the opportunity to reply regarding the patentability thereof. However, the Office Action of 7/14/2006 still failed to identify several elements and functional imitations recited in the claims. Additionally, the Office Action of 7/14/2006 failed to respond to several arguments raised by Applicant. Therefore, in the instant amendment, Applicant again requests the Examiner to identify several elements and functional limitations of *Beukema* relied upon by the Examiner as anticipating the limitations of the claims, reinstates many of the arguments, and respectfully requests the Examiner to respond thereto.

Claim 41

With respect to claim 41, the Examiner states in paragraph 47 of the Office Action of 11/18/2005 that *Beukema* teaches at least three data interfaces including the HCA and the TCA of the computer systems of *Beukema*'s Infiniband (IB) network. In the Office Action of 7/14/2006, the Examiner states that the three interfaces are an HCA interface, an I/O interface, and a TCA interface. Thus, Applicant assumes the Examiner is relying on at least three of the PCI interfaces and IB ports of the IB HCA, TCA, and I/O adapter

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[1] Claim 41 is the only claim for which the Examiner attempts to give any explanation beyond paragraph and Figure numbers.

190/192 of Fig. 1 of *Beukema* to correspond to the claimed at least three data interfaces, wherein at least one of the interfaces is a different type. The Examiner further states that *Beukema* teaches a memory shared by the data interfaces, referring to page 4, paragraph [0039]. Thus, Applicant assumes the Examiner is relying on the system memory 340 of Figure 3 (which is representative of system memories 132 and 142 of Figure 1) to correspond to the claimed shared memory. The Examiner states that paragraphs [0077] and [0082] teach that the data interfaces share the system memory 340.

Paragraph [0077] describes a portion of the flowchart of Figure 8, which illustrates a CPU 126 issuing a store command to a PCI I/O adapter 190 of Figure 1 over the IB SAN of Figure 1. An IB HCA coupled to the CPU responsively encapsulates the PCI transaction generated by the store command into an IB packet and transmits the packet over the IB SAN to an IB TCA. The TCA decodes the packet into a PCI transaction to the PCI I/O adapter on a PCI bus connecting the I/O adapter to the TCA. Paragraph [0082] describes the flowchart of Figure 10, which illustrates a PCI I/O adapter 190 of Figure 1 performing a DMA write[2] operation across the IB SAN of Figure 1 to a processor node system memory 132 of Figure 1, of which system memory 340 of Figure 3 is representative. The PCI I/O adapter issues a PCI write command to a PCI bus connecting the I/O adapter and the IB TCA. The IB TCA responsively encapsulates the PCI write command into an IB packet and transmits the packet over the IB SAN to an IB HCA. The HCA decodes the packet and creates a write operation to the system memory 340 with the data and address specified in the PCI write command in the packet.

Applicant respectfully requests the Examiner to specifically identify where *Beukema* teaches that at least three of the IB ports and PCI interfaces of the HCA, TCA, and I/O adapter share the system memory 340. Applicant respectfully asserts that, contrary to Applicant's request in the Amendment of 4/18/2006, the Examiner did not identify how the HCA, TCA, and I/O adapter interfaces share the system memory 340. Applicant can find no such teaching in any of the paragraphs or Figures of *Beukema* referred to by the

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[2] Although the first sentence of paragraph [0082] states "DMA read operation," the remainder of the paragraph states "DMA write operation" and obviously describes a DMA write operation by a PCI I/O adapter. In contrast, paragraph [0083] describes a DMA read operation by a PCI I/O adapter.

Examiner, nor in any other parts of *Beukema*. In particular, the PCI interface and IB port of the TCA cannot share the system memory since they are entirely on the other side of the SAN and are separated by various IB links and switches and the HCA itself. Furthermore, the IB ports of the HCA cannot share the system memory. Nowhere does *Beukema* teach the HCA IB ports sharing the system memory 340. Rather, the only HCA, TCA, or I/O adapter element that *Beukema* teaches can access the system memory 340 is the DMA function 340 of the HCA of Figure 3 (see page 4, paragraph [0039], last sentence), which uses the PCI interface of the HCA to transfer the data to the system memory 340. Thus, Applicant respectfully asserts that *Beukema* does not teach the claimed at least three data interfaces, at least one being of a different type than the others, (assumed to be at least three of the PCI interfaces and IB ports of the IB HCA and TCA) sharing the claimed memory (assumed to be system memory 340).

The Examiner further states that *Beukema* teaches a transaction switch that dynamically allocates portions of the shared memory to the data interfaces for storing data therein and controls access by the data interfaces to the allocated shared memory portions, referring to page 8, paragraph [0082]. Applicant cannot determine from paragraph [0082] which element of the network of *Beukema* the Examiner relies upon to correspond to the claimed transaction switch. Furthermore, contrary to Applicant's request in the Amendment of 4/18/2006, the Examiner has not identified where *Beukema* teaches the claimed transaction switch. In the clause of paragraph 47 of the Office Action regarding the shared memory, the Examiner states "there are plurality of DMA requests (read/write) send by plurality of hosts, the correct HCA is to dynamically allocate system memory to complete a DMA write operation." The statement by the Examiner appears to indicate that the Examiner is relying on the HCA to correspond to the claimed transaction switch that allocates portions of the system memory to the at least three data devices. Applicant can find no teaching in *Beukema* of the HCA (which Applicant assumes the Examiner is relying on to correspond to the claimed transaction switch) allocating system memory 340 and respectfully requests the Examiner to specifically identify where *Beukema* teaches this. Furthermore, one of ordinary skill in the art reading *Beukema* at the time the invention was made would understand that an operating system executing on the

processor node CPUs, not the HCA, would allocate portions of the system memory for use by the HCAs and CPUs of the processor node since the operating system manages the system memory resource, and *Beukema* does not teach anything contrary to this knowledge of an ordinarily skilled artisan. Thus, Applicant respectfully asserts that *Beukema* does not teach the claimed transaction switch that allocates portions of the memory to at least three data interfaces for storing data, wherein at least one of the interfaces is a different type, and that controls access to the allocated portions of the memory by each of the data interfaces.

The Examiner states with respect to claim 41 (as well as claim 1, 63, 71 and 80-82) that, "It would have been obvious to the person of ordinary skill in the art at the time of the invention to combine teachings of Beukema and Warmke because the teaching of Warmke to allow for VHDL language to program an ASIC chip would improve the scalability and mobility of Beukema by programming the digital logic into a single chip as opposed to implementation realized using a plurality of network components." Applicant respectfully disagrees. Whereas it is highly desirable to integrate a router as described in *Warmke* into a single ASIC, it is not desirable to integrate a SAN into a single ASIC because it would frustrate the fundamental purpose of having a SAN: to enable the end nodes of the SAN (such as the host processor nodes, RAID subsystem, and I/O Chassis shown in Figure 1 of *Beukema*) to reside in different physical locations and be connected via cables. Indeed, *Beukema* illustrates this when *Beukema* explicitly states the goal is to include the PCI I/O adapters into a SAN fabric. See page 1, paragraph [0006]. Therefore a person of ordinary skill in the art would not have been motivated to integrate the SAN of *Beukema* regardless of the scalability and mobility "improvements." Therefore, Applicant respectfully asserts that the Examiner has failed to make a *prima facia* case of obviousness by failing to supply a suggestion, teaching, or motivation to combine the *Beukema* and *Warmke* references. The Examiner responded: "the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious." Applicant respectfully asserts that the differences between *Beukema* and the claimed invention are not otherwise obvious.

For the reasons stated above, Applicant respectfully asserts that *Beukema* in view of *Warmke* does not obviate claim 41, and respectfully requests the Examiner to withdraw the rejection. Applicant respectfully asserts *Beukema* in view of *Warmke* does not obviate dependent claims 42-62 because they depend from independent claim 41, which is not obviated by *Beukema* in view of *Warmke* for the reasons discussed above.

Claim 36

Applicant has amended claim 36 to clarify that the control logic is coupled to the memory and the plurality of transaction queues.

With respect to claim 36, in the Office Action at paragraph 17, the Examiner states that *Beukema* teaches a memory shared by a plurality of data interfaces. Because the Examiner has not referred to any specific portions of *Beukema*, Applicant cannot determine which element of *Beukema* the Examiner is relying on to correspond to the claimed shared memory, and again respectfully requests the Examiner to specifically identify the relied-upon element. However, to further prosecution of the case, based on the Examiner's statements regarding claim 41 discussed above, Applicant assumes the Examiner is relying on the system memory 340 of Figure 3 to correspond to the claimed shared memory. Applicant appreciates the Examiner identifying in the Office Action of 7/14/2006 that the Examiner is relying on the queue pairs (QPs) of *Beukema* as corresponding to the claimed transaction queues.

Applicant respectfully asserts that the work queue elements (WQEs) taught by *Beukema* do not anticipate the claimed transactions and the QPs do not anticipate the claimed transaction queues since WQEs are not adapted to convey information to enable data interfaces to transfer data according to a plurality of disparate data transfer protocols. A person of ordinary skill in the art reading *Beukema* at the time the invention was made would know that IB QPs are used to transfer data, not according to a plurality of disparate data transfer protocols, but rather according to a single data transfer protocol, namely IB messages at the transport layer level from the IB transport layer on a local node to the IB transport layer on a remote node, as shown in Figure 25 of the Infiniband Architecture Specification Volume 1 Release 1.0 at page 91, which is incorporated by reference into

Applicant's application at page 18, lines 5-7, and which was reproduced from the Infiniband Specification in Applicant's Amendment of 4/18/2006. This is also consistent with what *Beukema* teaches, which is consistent with the fact that the Bruce Beukema, inventor of U.S. Patent Application 2002/0073257 (*Beukema*), and co-inventor Renato Recio are authors of the Infiniband Architecture Specification Volume 1 Release 1.0, as indicated at pages 31 and 32 of the IBA Specification, which was published approximately six weeks before the filing of U.S. Patent Application 2002/0073257 (*Beukema*). In particular, *Beukema* does not teach that WQEs are adapted to convey information to enable data interfaces to transfer data according to a plurality of disparate data transfer protocols. Rather, in paragraph [0042] *Beukema* explicitly states: "The method of using the SAN to send foreign protocols across the network, as defined herein, does not use the queue pairs, but instead bypasses these on the way to the SAN." Still further, *Beukema* explicitly states that the HCA determines the packet is <u>not</u> a QP operation in the process of determining that the packet includes the encapsulated PCI operation. See paragraph [0082], fifth sentence. That is, the PCI I/O adapter DMA write operation taught by *Beukema* in Figure 10 does not use QP's (nor do the DMA read operation taught in Figure 11, the processor store to the PCI I/O adapter taught in Figure 8, and the processor load from the PCI I/O adapter taught in Figure 9). Thus, even if WQE's were adapted to convey information to enable data transfer according to a plurality of disparate data transfer protocols, which they are not, *Beukema* explicitly states that he does not employ QPs to transfer his IB-packet-encapsulated PCI transactions between the PCI I/O adapter and the system memory, nor between the processor node CPU and PCI I/O adapter. Thus, Applicant respectfully asserts that *Beukema* does not teach the claimed plurality of transaction queues, associated with each of the plurality of data interfaces, configured to store transactions, in which the transactions are adapted to convey information to enable the plurality of data interfaces to transfer data according to a plurality of disparate data protocols supported thereby.

Finally, the Examiner states that *Beukema* teaches control logic that routes the data through the shared memory between the data interfaces and switches the transactions between the data interfaces, referring to paragraph [0082]. Applicant cannot discern from

the general reference to paragraph [0082] which element of *Beukema* the Examiner is relying on to correspond to the claimed control logic and again respectfully requests the Examiner to specifically identify same.

For the reasons stated above, Applicant respectfully asserts that *Beukema* does not anticipate claim 36, and respectfully requests the Examiner to withdraw the rejection. Applicant respectfully asserts *Beukema* does not anticipate dependent claims 37-40 because they depend from independent claim 36, which is not anticipated by *Beukema* for the reasons discussed above.

Claim 79

With respect to claim 79, in paragraph 22 of the Office Action, the Examiner states that *Beukema* teaches a buffer manager that allocates portions of the plurality of data devices access to the buffer memory, referring to page 4, paragraph [0039]. Again, since paragraph [0039] describes Figure 3, Applicant assumes the Examiner is relying on the system memory 340 of Figure 3 to correspond to the claimed buffer memory. Applicant cannot determine from the Examiner's reference broadly to paragraph [0039] which element of *Beukema* the Examiner is relying to correspond to the claimed buffer manager. Applicant again respectfully requests the Examiner to designate the particular part of *Beukema* relied upon as anticipating the claimed buffer manager, in order to provide Applicant the opportunity to reply regarding the patentability thereof. Again Applicant asserts, as stated above with respect to claim 36, that one of ordinary skill in the art reading *Beukema* at the time the invention was made would understand that an operating system executing on the processor node would manage the system memory resource and allocate access thereto, and *Beukema* does not teach anything contrary to this knowledge of an ordinarily skilled artisan.

The Examiner further states, referring to Figure 1, that *Beukema* teaches a plurality of data paths that provide the data devices access to the buffer memory. In the Office Action of 7/14/2006, the Examiner states that *Beukema* discloses in Figure 3 a plurality of paths coupled to the memory 340, for example a first path connected between memory 340 to port 312-316 and a second path connected between memory 340 to SMA "and so

on." Applicant respectfully points out that the claim recites that the data paths connect the shared memory to the packetized and addressed data devices. Applicant can find no teaching in *Beukema* that the SMA is a packetized or addressed data device. Furthermore, it is unclear to Applicant from Fig. 3 of *Beukema* that there are data paths connecting the memory 340 to the ports 312-316 and to the SMA. Therefore, Applicant respectfully asserts that *Beukema* does not teach the claimed data paths that couple the claimed buffer memory (assumed to be the system memory 340/132/142) and the claimed plurality of packetized and addressed data devices and provide the plurality of data devices access to the buffer memory.

The Examiner further states that *Beukema* teaches a mapping table that stores packet destination identification information, referring to page 7, paragraph [0077]. Additionally, the Examiner states[3] that "Beukema inherently teach a mapping table that operates within the routers [0022-0025], the routers knows the destinations of each transaction and would route the transaction along the network to their corresponding locations. The packets themselves have routing information embedded therein, the routers would know where to route the packets to the proper destinations based on such information (see [0077] and Fig 5, item 516, 518 and 510)." The Examiner also states that *Beukema* teaches a plurality of transaction queues that transfer transactions between the transaction switch and the data devices, referring to page 4, paragraphs [0039-0041]. For reasons similar to those discussed above with respect to claim 36, Applicant assumes the Examiner is relying on the QPs of Figure 3 to correspond to the claimed transaction queues and the WQEs of Figure 4 to correspond to the claimed transactions.

The Examiner also states that *Beukema* teaches control logic that selectively switches data between the plurality of data devices based on the mapping table information and in response to the transactions, referring to page 7, paragraph [0077] and page 8, paragraphs [0082] and [0084]. Paragraph [0084] describes a portion of the flowchart of Figure 11, which illustrates a PCI I/O adapter 190 of Figure 1 performing a DMA read operation

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[3] This is in the Office Action, on page 20, with respect to claim 79, in the paragraph beginning, "As to point C:". Although point C on page 19 states: "With respect to claim 63, …", apparently the Examiner is referring to claim 79 since claim 63 does not recite a mapping table, whereas claim 79 does recite a mapping table.

across the IB SAN of Figure 1 from a processor node system memory 132 of Figure 1, which is represented by memory 340 of Figure 3. The PCI I/O adapter issues a PCI read command to a PCI bus connecting the I/O adapter and the IB TCA. The IB TCA responsively encapsulates the PCI read command into an IB packet and transmits the packet over the IB SAN to an IB HCA. The HCA decodes the packet and creates a read operation from the system memory with the address specified in the PCI read command in the packet. The HCA receives the requested data from the system memory, encapsulates the data with a PCI Read Reply command in an IB packet including in its header the LID of the TCA that transmitted the first packet, and transmits the packet to the SAN, which routes the packet to the TCA. The TCA decodes the packet and provides the Read Reply including the data to the PCI I/O adapter.

Applicant cannot discern from the general reference to paragraphs [0077], [0082], and [0084] which element of *Beukema* the Examiner is relying on to correspond to the claimed control logic and again respectfully requests the Examiner to specifically identify the relied-upon element of *Beukema*. Furthermore, Applicant again respectfully requests the Examiner to identify how the relied-upon element of *Beukema* switches data between the packetized and addressed data devices based on mapping table information in the router 117 of Figure 1 and in response to transactions. Finally, Applicant again respectfully requests the Examiner to identify how the transaction queues transfer transactions between the transaction switch (Applicant also cannot discern which element of *Beukema* the Examiner is relying on to correspond to the transaction switch and again respectfully requests the Examiner to specifically identify it) and the packetized and addressed data devices. Nevertheless, Applicant observes that a person of ordinary skill in the art at the time of the invention would have known that IB routers, including the router 117 of Figure 1 of *Beukema*, do not switch data based on WQEs; rather, IB WQEs are only used by an IB consumer to communicate with IB channel adapters, not with IB switches or routers, and *Beukema* teaches nothing to the contrary.

For the reasons stated above, Applicant respectfully asserts that *Beukema* does not anticipate claim 79, and respectfully requests the Examiner to withdraw the rejection.

Claim 23

Applicant has amended claim 23 to clarify that the multiplexing logic is coupled to the shared memory and the control logic is coupled to the multiplexing logic.

With respect to claim 23, the Examiner states that *Beukema* teaches a memory shared by a plurality of data devices for buffering data received thereby, wherein the data devices comprise a plurality of packetized data devices and a plurality of addressed data devices, referring to paragraphs [0007], [0039-0041], and [0082] of *Beukema*. In the Office Action of 7/14/2006, the Examiner states that the ports 312-316, the SMA, and MTP of Fig. 3 share memory 340. As stated above, Applicant can find no teaching in *Beukema* that the SMA is a packetized or addressed data device. Furthermore, Applicant can find no teaching in *Beukema* that the MTP is a packetized or addressed data device. Thus, Applicant respectfully asserts that *Beukema* does not teach a memory shared by a plurality of data devices for buffering data received thereby, wherein the data devices comprise a plurality of packetized data devices and a plurality of addressed data devices.

Further with respect to claim 23, the Examiner states that *Beukema* teaches multiplexing logic that controls the transfer of data between the data devices and the shared memory, and control logic that controls the multiplexing logic to transfer data through the memory between two of the packetized data devices and between one of the packetized data devices and one of the addressed data devices, referring to paragraphs [0007], [0082], and [0084] of *Beukema*. Applicant cannot discern from the general reference to paragraphs [0007], [0082], and [0084] which elements of *Beukema* the Examiner is relying on to correspond to the claimed multiplexing logic and control logic and again respectfully requests the Examiner to specifically identify the relied-upon elements. Furthermore, Applicant respectfully requests the Examiner to identify how the relied-upon elements of *Beukema* perform the claimed controlling of the transfer of data through the shared memory (system memory 340) between the claimed two of the packetized data interfaces (ports 312-316) and through the claimed shared memory (system memory 340) between one of the packetized data interfaces (ports 312-316) and one of the addressed data interfaces (SMA and MTP).

For the reasons stated above, Applicant respectfully asserts that *Beukema* does not anticipate claim 23, and respectfully requests the Examiner to withdraw the rejection. Applicant respectfully asserts *Beukema* does not anticipate dependent claims 24-35 because they depend from independent claim 23, which is not anticipated by *Beukema* for the reasons discussed above.

Claim 1

With respect to claim 1, the Examiner states that *Beukema* teaches a bus router that performs transport layer operations between a plurality of IB MACs and a plurality of local bus interfaces, referring to paragraphs [0020] and [0024]. Paragraphs [0020] and [0024] describe a SAN. The SAN includes end nodes that transfer messages to one another via routers and switches that interconnect the end nodes and links that connect the end nodes, routers, and switches. Each message is transferred via one or more packets through the network. The end nodes may communicate using multiple paths through the network to achieve fault tolerance and increased data transfer bandwidth.

Applicant cannot clearly discern from the general reference to paragraphs [0020] and [0024] which element of *Beukema* the Examiner is relying on to correspond to the claimed bus router and again respectfully requests the Examiner to specifically identify the relied-upon element. Furthermore, Applicant respectfully requests the Examiner to identify how the relied-upon element of *Beukema* performs the claimed transport layer operations between the MACs and local bus interface. However, for the purpose of furthering prosecution Applicant again assumes that the Examiner is relying on the router 117 of Figure 1 to correspond to the claimed bus router, and respectfully requests the Examiner to confirm or deny this assumption. Given this assumption, Applicant can find no teaching in *Beukema* of the router 117 having a local bus interface; consequently, *Beukema* does not teach the router 117 performing transport layer operations between the MACs and local bus interface; rather, *Beukema* teaches the router 117 routing only packets and only between the IB ports, as shown in Figure 25. Therefore, Applicant respectfully asserts that *Beukema* does not teach a bus router (assumed to be the router

117 of Figure 1) performing transport layer operations between MACs and a local bus interface.

In the Office Action of 7/14/2006, the Examiner states that *Beukema* teaches an I/O interface at pg. 1, paragraph [0005] that corresponds to the claimed local bus interface. Applicant can find no teaching in paragraph [0005] of *Beukema* of a local bus interface. The only use of the terms "I/O" and "interface" used in paragraph [0005] are unconnected and are as follows. The first sentence of paragraph [0005] states: "In a SAN, the hardware provides a message passing mechanism which can be used for Input/Output devices (I/O) ...." The last sentence of paragraph [0005] states: "The software that interprets verbs and directly accesses the channel adapter is known as the channel interface (CI)." Applicant can find no teaching in these statements, or elsewhere in paragraph [0005] of a local bus interface on a network interface adapter, as recited in amended claim 1.

Further with respect to claim 1, the Examiner states that *Beukema* teaches a transaction switch that switches data and transactions between the IB MACs, local bus interfaces, and bus router, referring to paragraph [0082]. Applicant cannot clearly discern from the general reference to paragraph [0082] which element of *Beukema* the Examiner is relying on to correspond to the claimed transaction switch and again respectfully requests the Examiner to specifically identify the relied-upon element. However, for the purpose of furthering prosecution Applicant assumes that the Examiner is relying on the switches 112/114 of Figure 1 to correspond to the claimed transaction switch, and respectfully requests the Examiner to confirm or deny this assumption. Given this assumption, Applicant can find no teaching in *Beukema* of the switches 112/114 having a local bus interface; consequently, *Beukema* does not teach the switches 112/114 switching data and transactions between MACs, a local bus interface, and a bus router; rather, *Beukema* teaches the switches 112/114 switching only packets and only between IB ports, as shown in Figure 25. Therefore, Applicant respectfully asserts that *Beukema* does not teach a transaction switch (assumed to be the switches 112/114 of Figure 1) that switches data and transactions between the MACs, local bus interface, and bus router.

For the reasons stated above, Applicant respectfully asserts that *Beukema* in view of *Warmke* does not obviate claim 1, and respectfully requests the Examiner to withdraw the rejection. Applicant respectfully asserts *Beukema* in view of *Warmke* does not obviate dependent claims 2-22 because they depend from independent claim 1, which is not obviated by *Beukema* in view of *Warmke* for the reasons discussed above.

Claim 63

The Examiner rejected claim 63 for the same reasons claim 1 was rejected. For reasons similar to those discussed above with respect to claim 1, Applicant respectfully asserts that *Beukema* does not teach the invention recited in claim 1. Furthermore, if the Examiner maintains the rejection, Applicant again respectfully requests the Examiner to specifically identify which element of *Beukema* the Examiner is relying upon to correspond to the claimed transaction switch.

For the reasons stated above, Applicant respectfully asserts that *Beukema* in view of *Warmke* does not obviate claim 63, and respectfully requests the Examiner to withdraw the rejection. Applicant respectfully asserts *Beukema* in view of *Warmke* does not obviate dependent claims 64-66 because they depend from independent claim 63, which is not obviated by *Beukema* in view of *Warmke* for the reasons discussed above.

Claim 67

The Examiner rejected claim 67 for the same reasons claims 1 and 2 were rejected. For reasons similar to those discussed above with respect to claim 1 and claim 36, Applicant respectfully asserts that *Beukema* does not teach the invention recited in claim 67. Furthermore, if the Examiner maintains the rejection, Applicant again respectfully requests the Examiner to specifically identify which elements of *Beukema* the Examiner is relying upon to correspond to the claimed transport layer engine, transaction queues, and transaction switch.

For the reasons stated above, Applicant respectfully asserts that *Beukema* in view of *Warmke* does not obviate claim 67, and respectfully requests the Examiner to withdraw the rejection. Applicant respectfully asserts *Beukema* in view of *Warmke* does not obviate

dependent claims 68-70 because they depend from independent claim 67, which is not obviated by *Beukema* in view of *Warmke* for the reasons discussed above.

Claim 71

The Examiner rejected claim 71 for the same reasons claim 1 was rejected. For reasons similar to those discussed above with respect to claim 1, Applicant respectfully asserts that *Beukema* does not teach the invention recited in claim 71.

For the reasons stated above, Applicant respectfully asserts that *Beukema* in view of *Warmke* does not obviate claim 71, and respectfully requests the Examiner to withdraw the rejection. Applicant respectfully asserts *Beukema* in view of *Warmke* does not obviate dependent claims 72-78 because they depend from independent claim 71, which is not obviated by *Beukema* in view of *Warmke* for the reasons discussed above.

Claims 1, 41, 63, 71 and 80-82

The Examiner states with respect to claims 1, 41, 63, 71 and 80-82 that, "It would have been obvious to the person of ordinary skill in the art at the time of the invention to combine teachings of Beukema and Warmke because the teaching of Warmke to allow for VHDL language to program an ASIC chip would improve the scalability and mobility of Beukema by programming the digital logic into a single chip as opposed to implementation realized using a plurality of network components." Applicant respectfully disagrees. Whereas it is highly desirable to integrate a router as described in *Warmke* into a single ASIC, it is not desirable to integrate a SAN into a single ASIC because it would frustrate the fundamental purpose of having a SAN: to enable the end nodes of the SAN (such as the host processor nodes, RAID subsystem, and I/O Chassis shown in Figure 1 of *Beukema*) to reside in different physical locations and be connected via cables. Indeed, *Beukema* illustrates this when *Beukema* explicitly states the goal is to include the PCI I/O adapters into a SAN fabric. See page 1, paragraph [0006]. Therefore a person of ordinary skill in the art would not have been motivated to integrate the SAN of *Beukema* regardless of the scalability and mobility "improvements." Therefore, Applicant respectfully asserts that the Examiner has failed to make a *prima facia* case of obviousness by failing to supply a suggestion, teaching, or motivation to combine the

Beukema and *Warmke* references. For these reasons, in addition to the other reasons discussed above, Applicant respectfully requests that the Examiner withdraw his rejection to claims 1, 41, 63, 71, and 80-82 and any claims that depend from them.

SUMMARY OF REQUESTED INFORMATION FROM THE EXAMINER

In order to enable Applicant to fully reply regarding the patentability of the invention, Applicant summarizes the above requests of the Examiner.

A. IDENTIFYING ELEMENTS AND FUNCTIONAL LIMITATIONS

Applicant respectfully requests the Examiner, where at all possible, to state the element(s) of *Beukema* by reference numeral(s) and name(s) that correspond to the element recited in the claims, and to state the text of *Beukema* by line number(s) within the paragraphs that teach the functional limitations recited in the claims. Applicant recognizes that the *Beukema* publication does not include line numbers in the margins, but requests the Examiner to assume the first line of a paragraph is "line 1", the second line of the paragraph is "line 2", and so forth. The elements and functional limitations are listed here by claim.

Claim 41

1. Please identify which element in *Beukema* corresponds to the <u>transaction switch</u>.
   Specifically, is the HCA 102 of Fig. 1 the transaction switch?

Claim 36

1. Please identify which element in *Beukema* corresponds to the <u>control logic</u> that routes
   data through the shared memory between the data interfaces and switches
   transactions between the data interfaces.

Claim 79

1. Please identify which element in *Beukema* corresponds to the <u>buffer manager</u>.

2. Please identify which element in *Beukema* corresponds to the <u>control logic</u> that selectively switches data between the data devices based on mapping table information and in response to transactions.

3. Please identify the text of *Beukema* that teaches <u>how</u> *Beukema*'s control logic element (whatever is identified in the previous question) <u>selectively switches data between the data devices based on the mapping table information and in response to transactions</u>.

4. Please identify the text of *Beukema* that teaches <u>how</u> *Beukema*'s queue pairs (QPs) <u>transfer</u> work requests (WQEs) <u>between the transaction switch and the data devices</u>.

<u>Claim 23</u>

1. Please identify which element in *Beukema* corresponds to the <u>multiplexing logic and control logic</u>.

2. Please identify the text of *Beukema* that teaches <u>how</u> *Beukema*'s multiplexing and control logic elements (whatever are identified in the previous question) control the transfer of data through the shared memory between the two packetized data interfaces and through the shared memory between one of the packetized data interfaces and one of the addressed data interfaces.

<u>Claim 1</u>

1. Please identify which element in *Beukema* corresponds to the <u>bus router.</u> Specifically, is the router 117 of Fig. 1 the bus router?

2. The Examiner states that paragraph [0005] teaches an I/O interface. What lines of paragraph [0005] is the Examiner referring to that teach a local bus interface?

3. Please identify which element in *Beukema* corresponds to the <u>transaction switch.</u> Specifically, are the switches 112/114 of Fig. 1 the transaction switch?

<u>Claim 63</u>

1. Please identify which element in *Beukema* corresponds to the <u>transaction switch</u>.

Claim 67

1. Please identify which elements in *Beukema* correspond to the <u>transport layer engine</u> and the <u>transaction switch</u>.

Claim 77

1. At which lines of paragraph [0007] does *Beukema* teach performing protocol translation in a transfer of data between a packetized data interface and a addressed data interface <u>without double-buffering the data</u>, as the Examiner states in the Office Action of 11/18/2005?

B. RESPONDING TO ARGUMENTS

Additionally, in Applicant's Amendment of 4/18/2006, Applicant presented several arguments that the Examiner did not respond to. Therefore, Applicant respectfully requests the Examiner/Supervisor to respond to the following arguments in the next Office Action.

Claim 41

1. The PCI interface and IB port of the TCA cannot share the system memory since they are entirely on the other side of the SAN and are separated by various IB links and switches and by the HCA itself. The Examiner states in the Response to Arguments of the most recent Office Action that three data interfaces are the HCA, TCA, and IOA. How do the HCA, TCA, and IOA "share" the system memory 340? In what sense do they share it?

2. An operating system executing on the processor node CPUs, not the HCA, would allocate portions of the system memory for use by the HCAs and CPUs of the processor node since the operating system manages the system memory resource.

Claim 36

1. IB QPs are used to transfer data, not according to a plurality of disparate data transfer protocols, but rather according to a single data transfer protocol, namely IB

messages at the transport layer level from the IB transport layer on a local node to
the IB transport layer on a remote node.

2. In paragraph [0042] *Beukema* explicitly states: "The method of using the SAN to send
foreign protocols across the network, as defined herein, does not use the queue
pairs, but instead bypasses these on the way to the SAN." Still further, *Beukema*
explicitly states that the HCA determines the packet is <u>not</u> a QP operation in the
process of determining that the packet includes the encapsulated PCI operation.
See paragraph [0082], fifth sentence.

<u>Claim 79</u>

1. IB routers, including the router 117 of Figure 1 of *Beukema*, do not switch data based
on WQEs; rather, IB WQEs are only used by an IB consumer to communicate
with IB channel adapters, not with IB switches or routers, and *Beukema* teaches
nothing to the contrary.

<u>Claim 23</u>

1. Applicant can find no teaching in *Beukema* of the transfer of data through the system
memory 340 between the IB port of the HCA and the IB port of the TCA. Rather,
in each of the DMA write, DMA read, processor store, and processor load
described in Figures 8-11 of *Beukema*, the data does not pass through the system
memory 340 between the HCA IB port and TCA IB port; rather, the system
memory 340 is either the source or destination of the data transferred. Similarly,
there is no teaching in *Beukema* of the transfer of data through the system
memory 340 between the IB port of the HCA or TCA and the PCI interface of the
HCA or TCA. Rather, in each of the DMA write, DMA read, processor store, and
processor load described in Figures 8-11 of *Beukema*, the data does not pass
through the system memory 340 between the HCA or TCA IB port and HCA or
TCA PCI interface, rather the system memory 340 is either the source or
destination of the data transferred.

<u>Claim 1</u>

1. Applicant can find no teaching in *Beukema* of the router 117 having a local bus

   interface; rather, *Beukema* teaches the router 117 routing <u>only packets</u> between

   the IB ports.

<u>**CONCLUSIONS**</u>

In view of the arguments advance above, Applicant respectfully submits that claims 1-113 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

Respectfully submitted,

/E. Alan Davis/

By:_____

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11/14/2006

Date: _____